Advanced Analog Integrated Circuits

Interference

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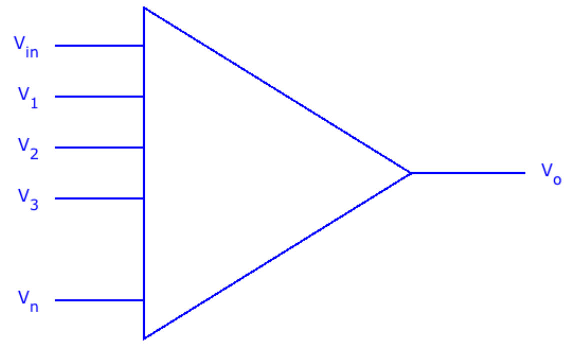
Interference



$$V_o = a_{in} \cdot V_{in} + \sum_i a_i V_i$$

a_{in} ↑ high

a_i ↑ ϕ

Typical Interferers

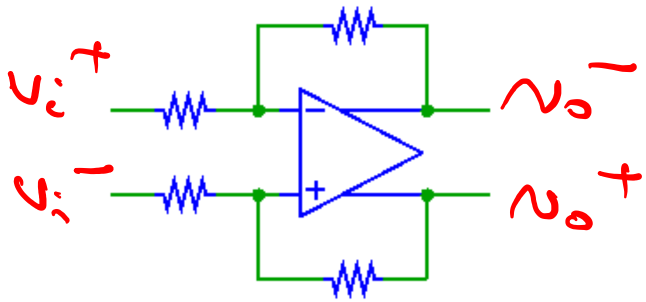
E.g.

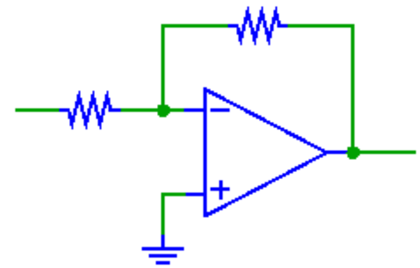
- Power supply
- Clocks
- Dig. circuits
- Power main 50/60 Hz, on PCBs

Coupling mech:

- C ⇐ IC
- L ⇐ PCB, bond wires

Fully Differential versus Single Ended





$$v_{id} = v_i^+ - v_i^- \leftarrow \text{signal}$$

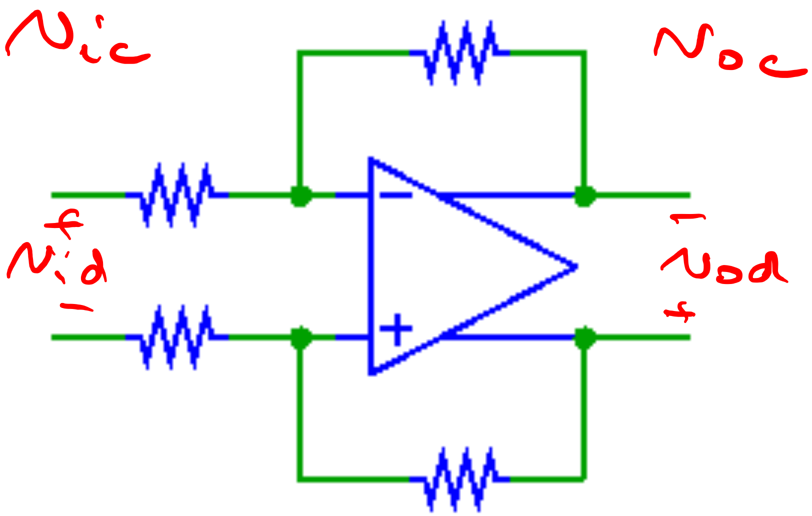
$$v_{ic} = \frac{v_i^+ + v_i^-}{2} \leftarrow \text{bias}$$

- symmetry
- inversion
- CMFB

- lower compl.
- needs amp
- No,

Is a Fully Differential Solution Required?

Differential versus Common-Mode



$$A_{dm} = \frac{v_{od}}{v_{id}} \rightarrow \infty$$

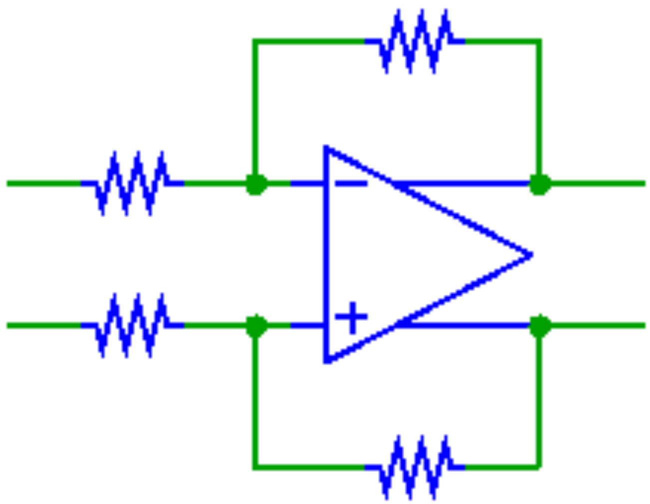
$$A_{cm} = \frac{v_{oc}}{v_{ic}} \rightarrow 0$$

$$A_{cdm} = \frac{v_{od}}{v_{ic}} \rightarrow 0$$

$$A_{vDD} = \frac{v_{od}}{v_{DD}} \rightarrow 0$$

$$A_{vSS} = \frac{v_{od}}{v_{SS}} \rightarrow 0$$

CMRR and PSRR

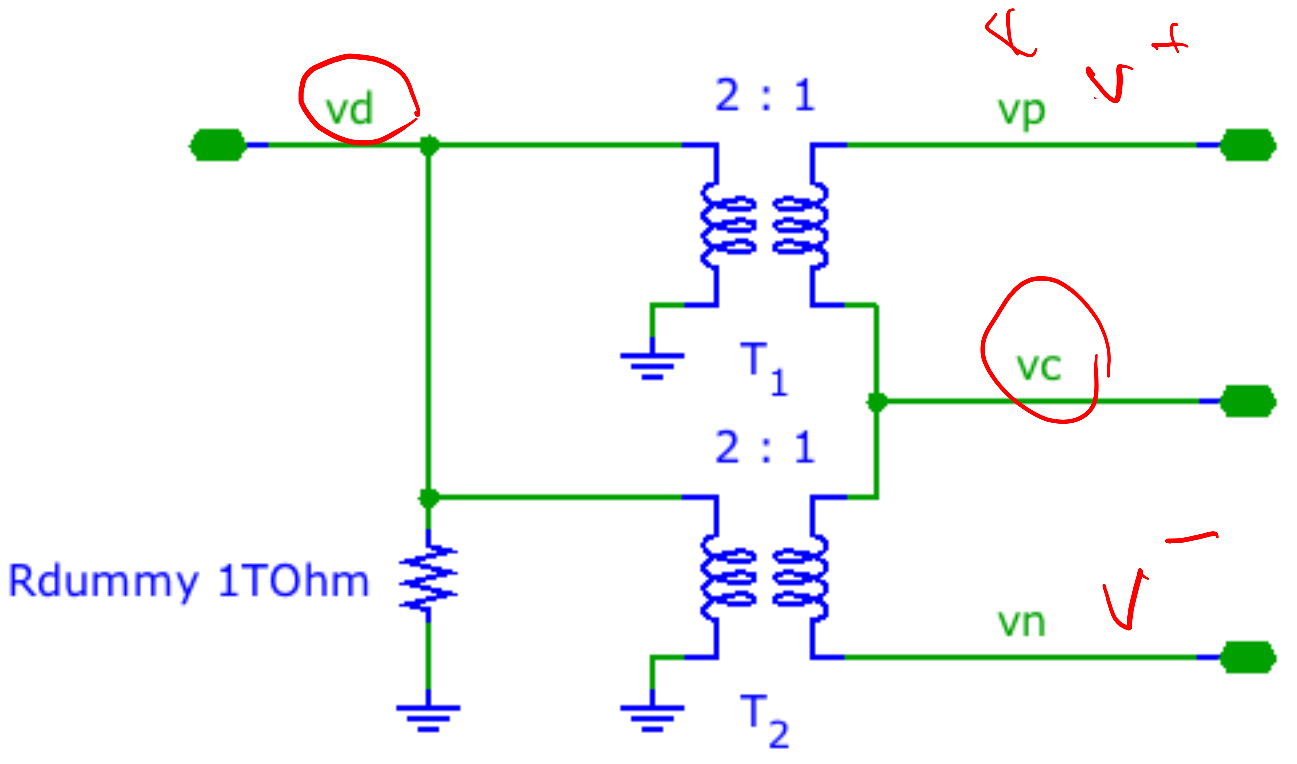


$$CMRR_{cd} = \left| \frac{A_{dm}}{A_{cdm}} \right| \to \infty$$

$$CMRR_{cc} = \left| \frac{A_{dm}}{A_{cm}} \right| \to \infty$$

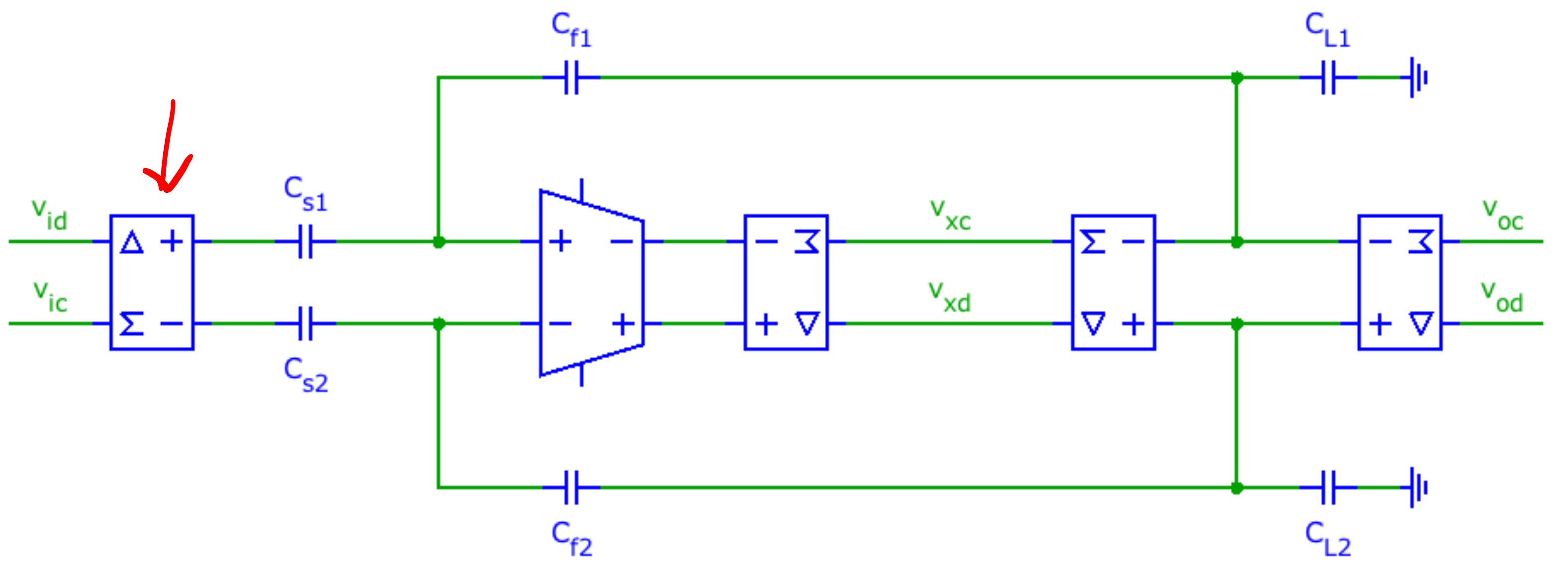
$$PSRR_{V_{DD}} = \left| \frac{A_{dm}}{A_{V_{DD}}} \right| \to \infty$$

Conversion: Balun



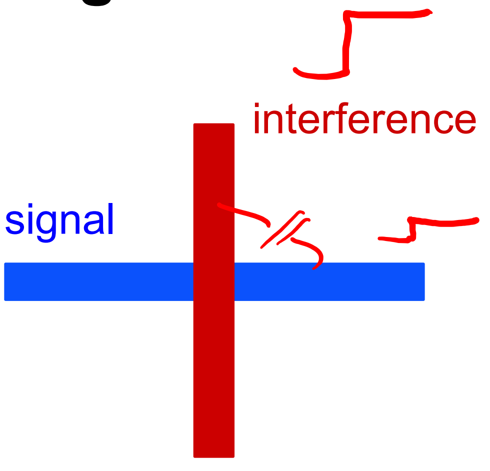
- Use for simulation only
- Realizable transformers inadequate for implementation at mixed-signal frequencies

Loop-Gain Simulation

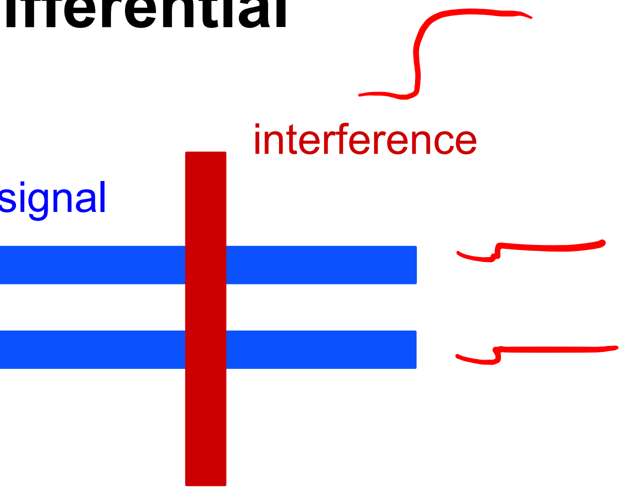


Interference Comparison

Single Ended



Differential



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Differential Pair

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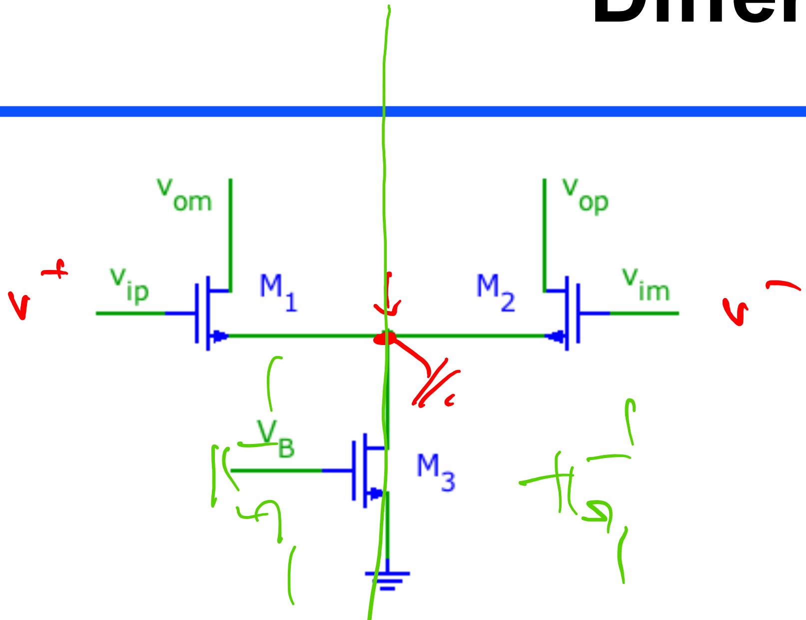
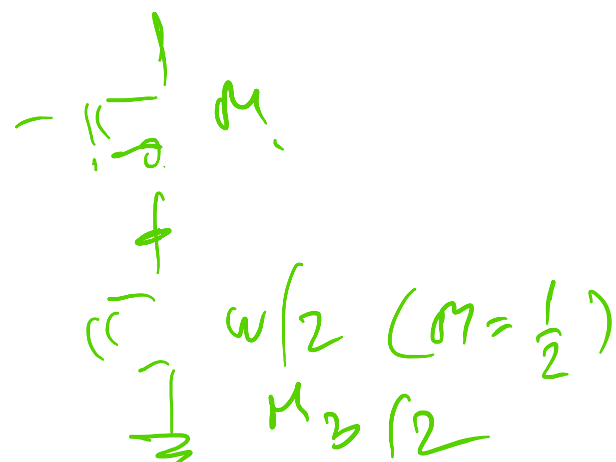
Differential Pair

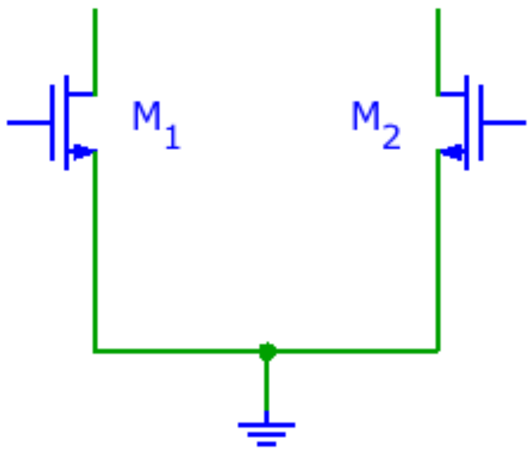


Differential Half Circuit

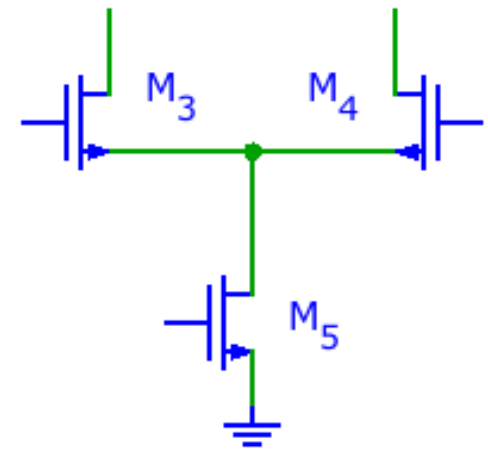
Common-Mode Half Circuit



Tail Current Source



versus



- higher swing
- I_B set by v_{ic}
- CMRR ?

- lower
- const bias
- good CMRR
- cascode

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Common-Mode Feedback

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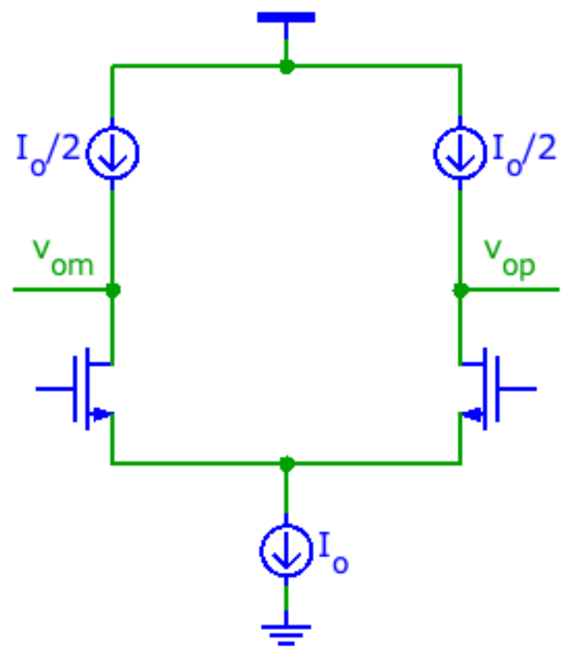
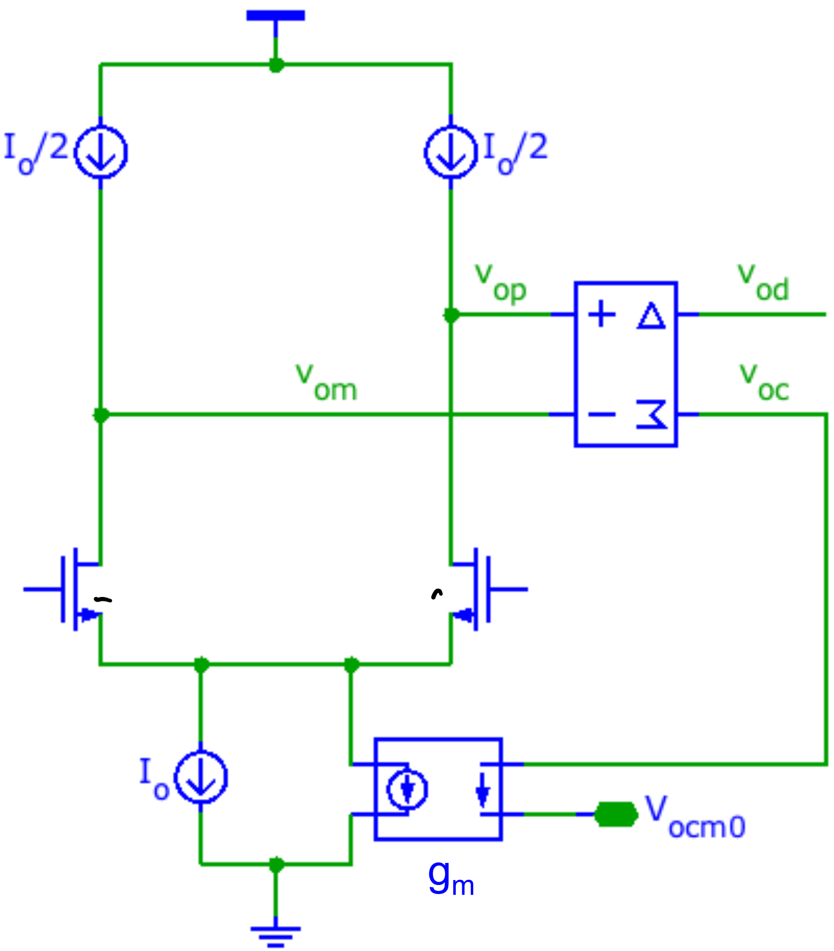
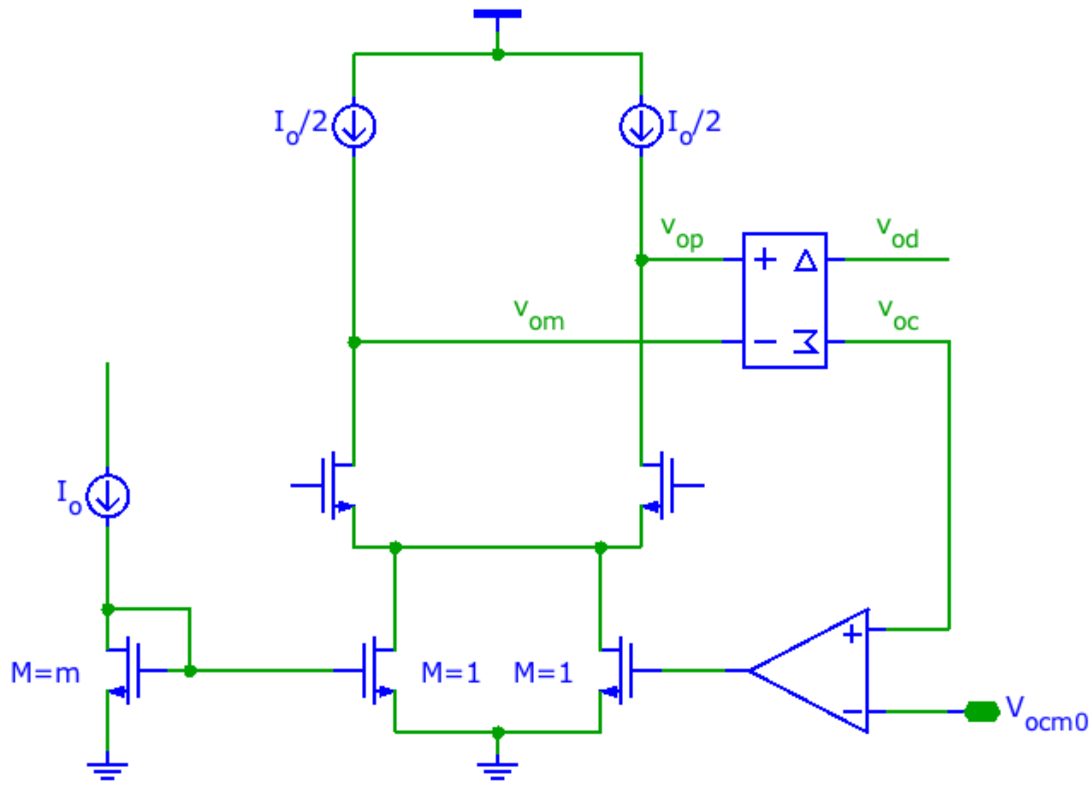
Output Common-Mode Voltage



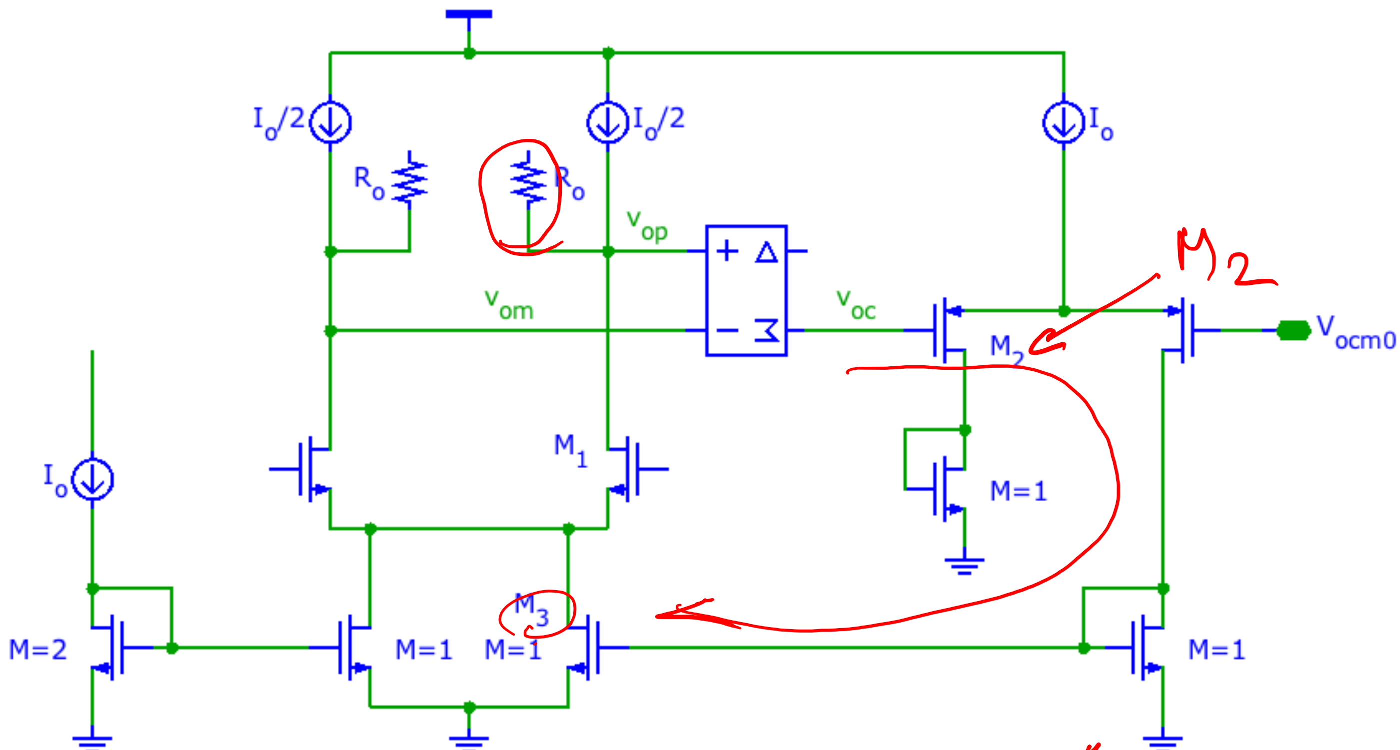
Common Mode Feedback (CMFB)



Realization: Adjusting V_{oc}

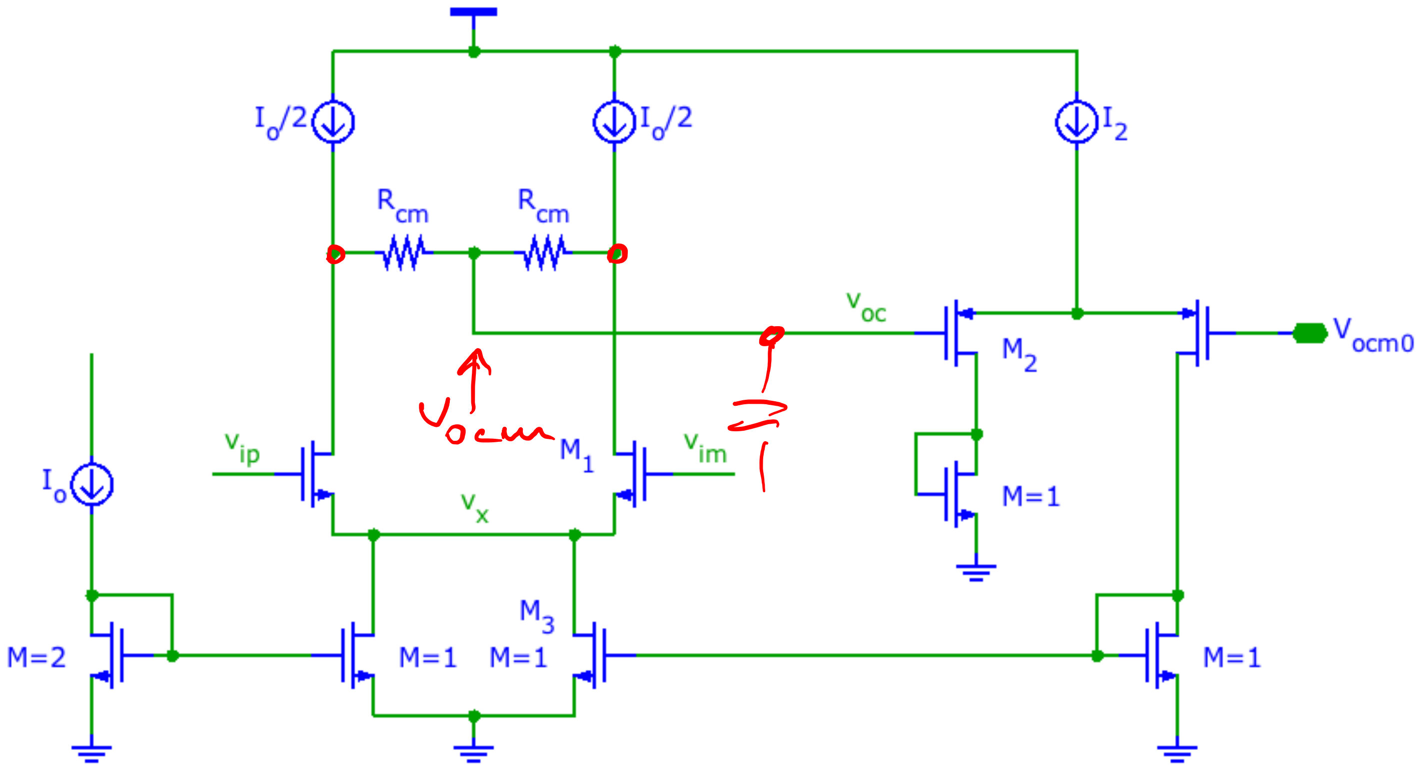


Controller



$$T_{o,cm} = \frac{g_{m3}}{2} \cdot R_o \cdot \frac{g_{m2}}{g_{m3}} = \underbrace{g_{m1} \cdot R_o}_{A_{dm}} \cdot \frac{g_{m3}}{2 g_{m1}}$$

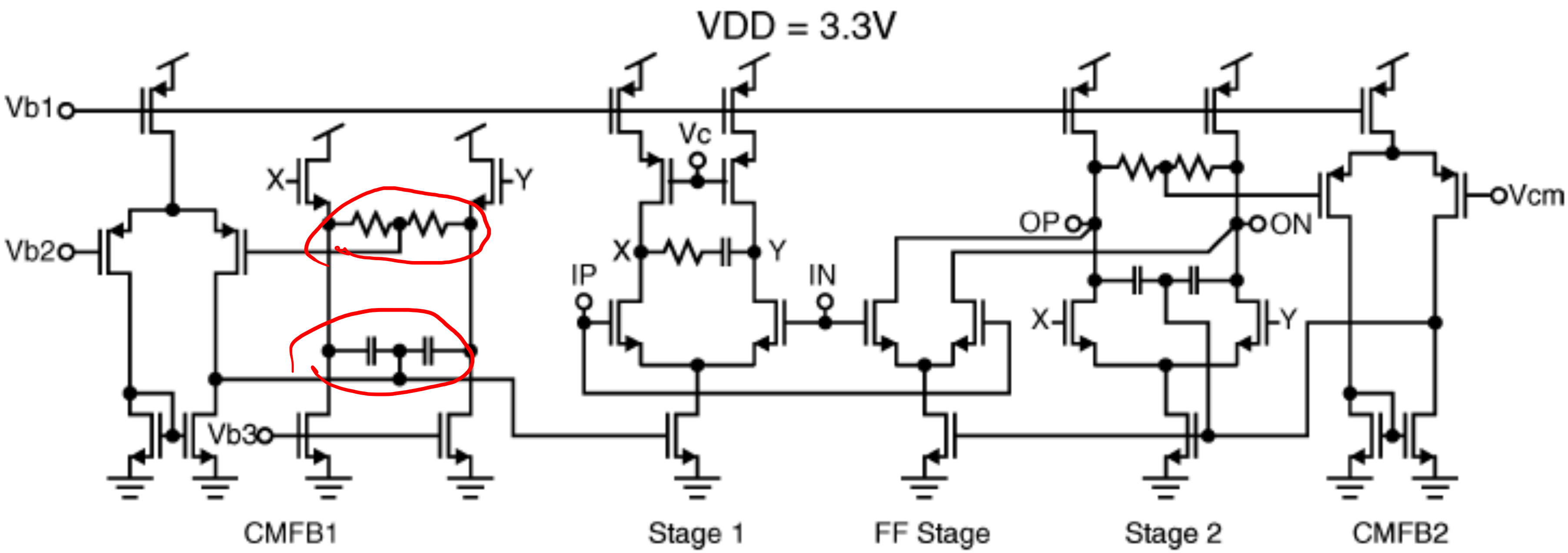
V_{cm} Sense



Adm ?

Beware of large Rcm

Continuous Time CMFB



Ref: R. Schreier et al., “A 375-mW quadrature bandpass ΔΣ ADC with 8.5-MHz BW and 90-dB DR at 44 MHz,” IEEE JSSC, Dec. 2006, pp. 2632-40.

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Switched Capacitor CMFB

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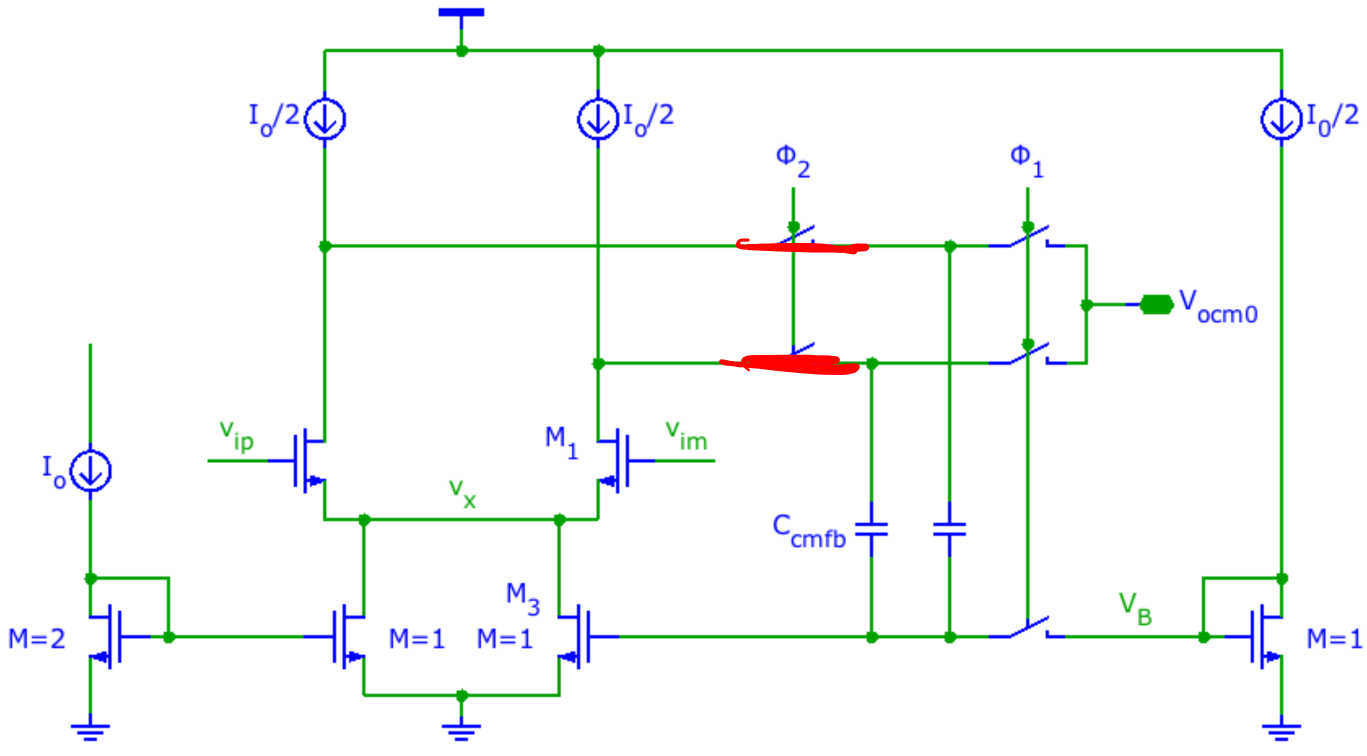
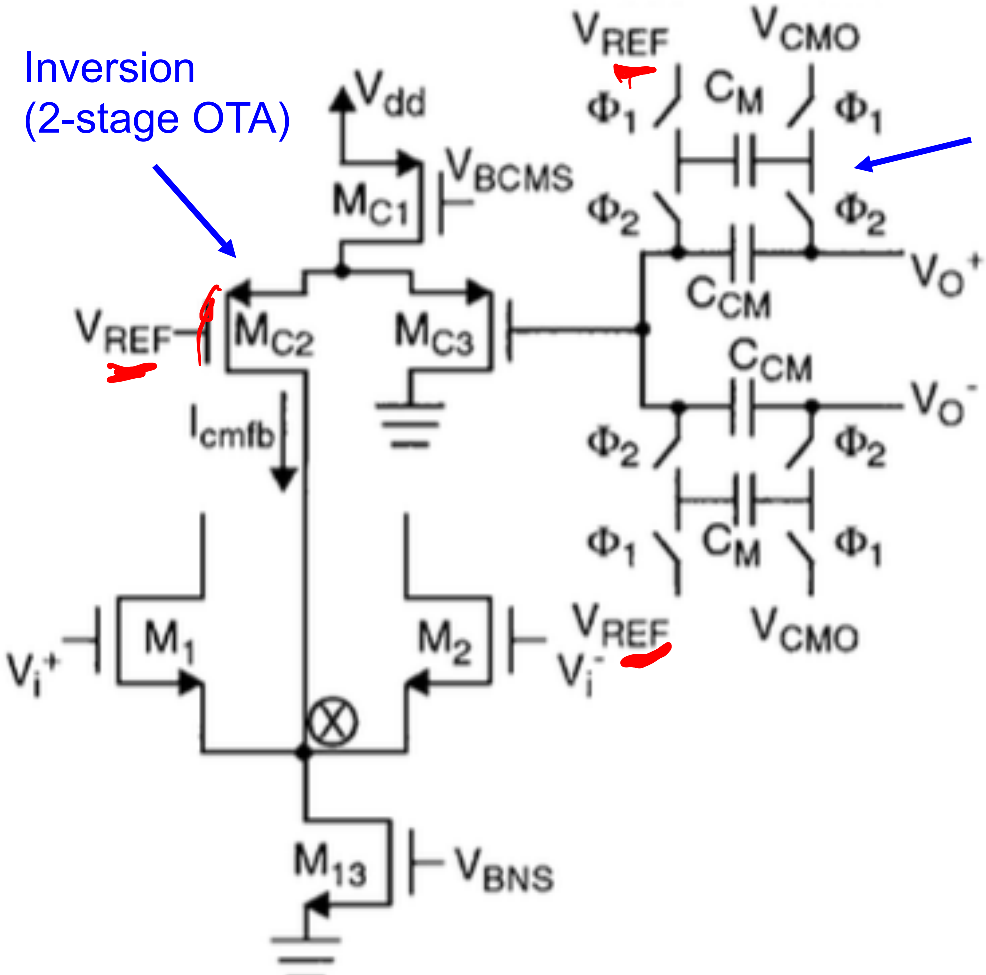
SC Common-Mode Feedback



Continuous SC CMFB

Inversion
(2-stage OTA)



Capacitive refresh, $C_M < C_{CM}$

$C_M << C_{CM}$

Ref: A. Feldman et al, "A 13 bit, 1.4 MS/s, 3.3 V sigma-delta modulator for RF baseband channel applications," JSSC Oct. 1998, pp. 1462-69.

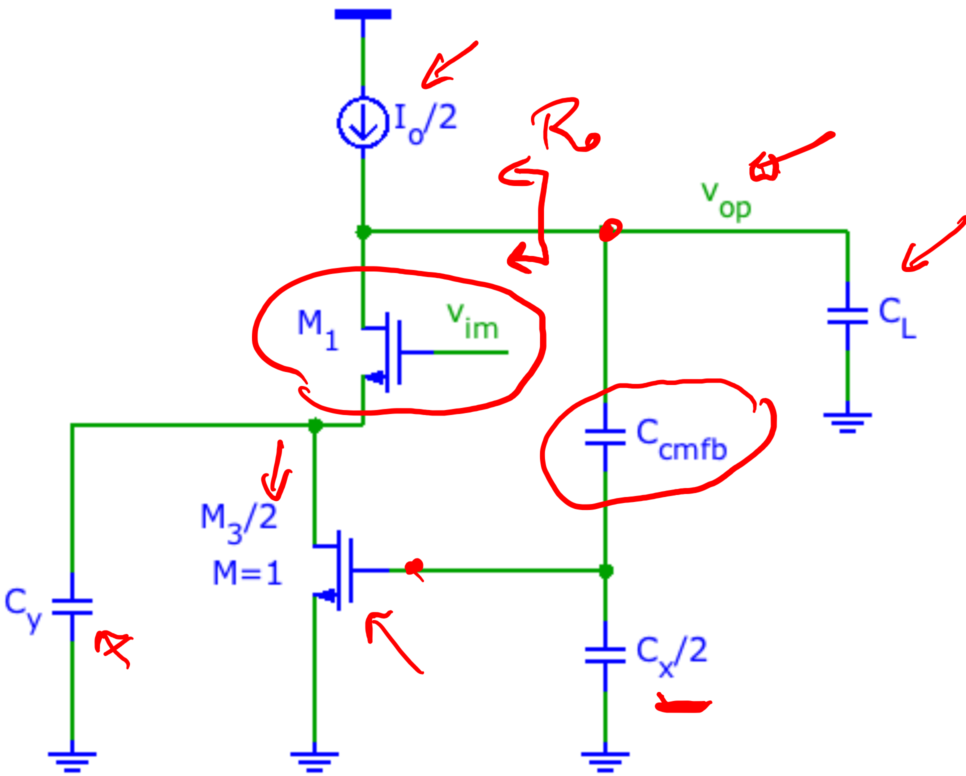
SC CMFB in 2-Stage Opamps

- 2 inversions

  (1) inverting amp
  1 tail CS

  (2) 2 CMFB circuits
  2 tail CS

CMFB Loop Gain



CMFB half circuit

$$T_o = \frac{g_{m3}}{2} \cdot R_o \cdot \frac{C_{cmfb}}{C_{cmfb} + \frac{C_x}{2}}$$

$$\omega_u \cong X \cdot \frac{g_{m3}/2 \, X}{C_L + \left(C_{cmfb} \parallel \frac{C_x}{2}\right)}$$

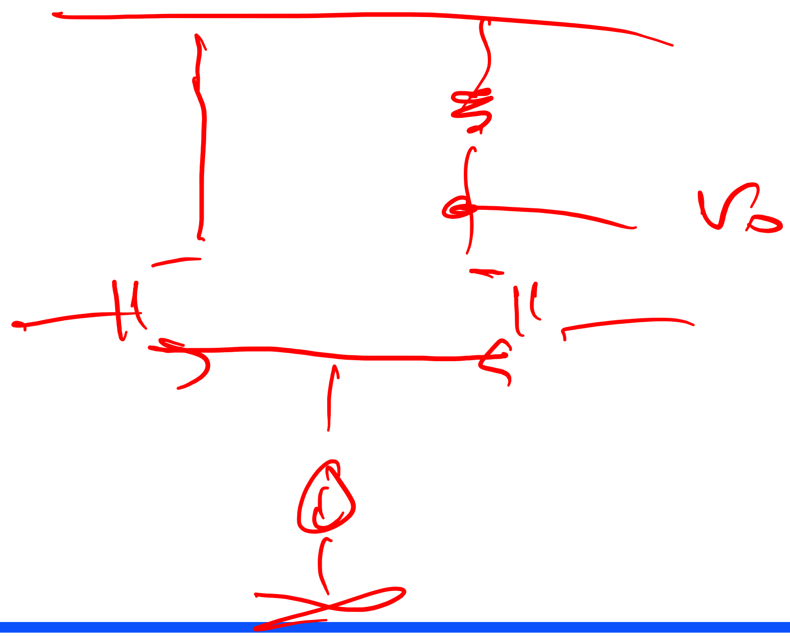
$$\omega_{nd} \cong \frac{g_{m1}}{C_y}$$

Setting the Loop Gain

- 2 coupled FB loops:
  (1) diff (2) cm
  CMFB
- BW needed depends on imbalance during transients
  → XTRs are nonlinear!
- Rule of thumb: $\omega_{u,cm\,fb} \cong \omega_{u,diff}/3$
  - Main amp settles to 10τ 2 … 3
    CMFB amp: 3 … 5τ
    ⇒ ~ 95% settling accuracy.
- Verify!

Noise in Differential Circuits

- 2x devices ⇒ 2x noise !
- But signal range doubles, too
  signal power: 4x power
  +3dB ! for 2x power dis



vs 3dB penalty!

Noise from Tail Current Source

If balanced:

rejected by CMRR

of next stage.